11.3 A Phase-Noise Reduction Technique for Quadrature LC-VCO with Phase-to-Amplitude Noise Conversion

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Quadrature phase clocking finds application in many communication systems. For RF front-ends, quadrature clocks are required for image rejection receivers and for down-converting RF/IF to baseband. For high-speed CDR systems, quadrature phase is required for half-rate phase detection, phase interpolation, and frequency detection.

Coupled quadrature VCOs (QVCOs) [1]-[2] operate away from the resonant frequency to create the required phase shift, which penalizes their FOM. Super-harmonic-coupled (SHC) QVCOs [3]-[4] do not have this problem, but they are not particularly effective in reducing phase noise.

Figure 11.3.1 shows the proposed energy-circulating QVCO. Two copies of complementary differential VCOs (DVCOs) are combined together at NMOS and PMOS tail nodes by two separate LC tanks. The oscillation waveform is shown in Fig. 11.3.2. The DVCOs produce quadrature phase outputs at frequency f_o. The transistors in a cross-coupled pair take turns operating in triode mode to pull the tail nodes up and down, creating waveforms at frequency $2f_o$. Transistor resistance in triode mode needs to be sufficiently low to drive the tail node capacitance such that $[2\pi R_{on}(V_{gs}=V_{DD})C_{tail}]^{-1} > 2f_o$; otherwise, it will fail to generate quadrature phase. The center-taps of the tail tank inductors L3 and L4 are connected to V_{DD} and ground through L5 and L6. The inductance of L5/L6 needs to be at least a few times higher than L3/L4 to prevent super-harmonic current shorting to V_{DD} and ground; bond wires can be employed to reduce the layout area, if it is a priority. An anti-phase relationship is forced at tail nodes CM1/CM2 and CM3/CM4 to yield 90° phase offset at f_o. Digital capacitor banks are used in the main and tail tanks to improve frequency tracking across the entire tuning range. Fine-tune varactors are used only in the main tanks.

Cross-coupled pairs act as bi-directional gateways converting f_o to $2f_o$ and $2f_o$ to f_o and allow energy to circulate among the main and tail tanks. The frequency f_o is actually lower than $1/\sqrt{LC}$ of the main tanks because the inductor current in the main tank not only flows into the capacitors of the main tank but also into the capacitors and inductors of the tail tanks, making the effective capacitance larger than the actual capacitance. Thermal noise is attenuated by the larger effective capacitance as well. For the two experimental designs presented, f_o is only 66% of $1/\sqrt{LC}$, which indicates the tight integration of main and tail tanks as an inseparable system.

Depending on the effectiveness of the coupling, a QVCO can reduce the phase noise by up to 3dB while doubling the power consumption in comparison to a stand-alone DVCO. This reduction cannot be realized with coupled QVCOs because strong coupling forces QVCOs to operate away from the resonant frequency, which increases the phase noise. Due to the large amount of energy circulating among the LC tanks, the proposed coupling method is more effective than SHC-QVCOs [3]-[4].

The proposed technique needs wider transistors than are necessary for a stand-alone DVCO, and one may suspect that the increased g_m would increase the noise injected into the system. This is not the case however; since the voltages at the tail nodes swing up and down, causing the transistors V_{gs}'s and g_m's to drop near the zero-crossings, reducing the injected noise. When a transistor enters the deep triode region its resistance is approximately 30× lower than the impedance of the main and tail tanks combined together at f_o and $2f_o$. As shown in Fig. 11.3.3, only a fraction of the available noise power from a triode-region transistor can be injected into the system due to the impedance mismatch. In contrast, a transformer-based SHC-QVCO [3] has better impedance matching at $2f_o$, which increases noise injection at $2f_o$.

We now examine the mechanism for further phase noise reduction. As shown in Fig. 11.3.3, the switch transistors inject little noise near f_o and $2f_o$ when they are off or in the triode region. As a result, the injected noise has been shaped with peak amplitude appearing near the zero-crossings of a DVCO. When the noise travels through the tail tanks to disturb the other DVCO, most of it is translated to amplitude noise, and is removed by the built-in amplitude limiting mechanism. This operation effectively desensitizes the phase noise response. Whenever there is a phase imbalance between the two DVCOs, phase noise in one DVCO is converted to amplitude noise in the other DVCO by the same mechanism.

The first test chip is intended for wireless applications that require wide tuning range for channel selection. It provides a 17% tuning range centered at 5.1GHz with 21 digital tuning keys and 2% continuous tuning in each key. The second test chip is targeted for fiber-optic transceivers and has a 1% continuous tuning range near 5.3GHz. The capacitances of the tail tanks are chosen to be half that of the main tanks to maximize inductor Qs while keeping the layouts manageable. Figure 11.3.4 shows the simulated phase noise of previous QVCOs and DVCOs relative to that of the first chip at 1MHz offset. The results shown are normalized to reflect the FOM differences:

$$L^*\{\Delta\omega\} = L\{\Delta\omega\} - 10\log\left[\left(\frac{f_o}{f_{o,ref}}\right)^2 \frac{P_{ref}}{P}\right] - L_{ref}\{1MHz\}$$

The same inductor models were used in all cases and capacitances were adjusted as necessary to make the oscillation frequencies close to 5GHz while maintaining the same tank Qs. The simulated FOM is 4.7dB better than a DVCO with noise filtering [5] and 3.1dB better than a DVCO biased by an ideal current source at its tail node. This result demonstrates the effectiveness of this technique in achieving better FOM and significantly lower phase noise than a stand-alone DVCO. The cause of any I/Q mismatch is dominated by the capacitance mismatch in the two main tanks. A capacitance mismatch of 1% causes 1.3° of I/Q mismatch.

Plots of the phase noise for both chips are shown in Fig. 11.3.5; they achieve -132.6dBc/Hz and -134.4dBc/Hz at 1MHz offset while consuming 27.7 and 20.7mW, respectively. The FOMs at 2MHz offset are 192 and 196dB, respectively. Figure 11.3.6 shows the performance summary and comparison to other published QVCOs. Even though the two designs are optimized for low phase noise instead of low FOM, the FOMs are at least 5.8dB better than prior work. Figure 11.3.7 shows the micrographs.

Acknowledgement:
This work was supported by UC MICRO Grants 03-094 and 04-101, Analog Devices, Broadcom, and Maxim Integrated Products. Chip fabrication was supported by TSMC.

References:
[1] P. Andreani and X. Wang, "On the Phase-Noise and Phase-Error Performances of Multiphase LC CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1883-1893, Nov., 2004.
[2] M. Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1018–1024, July, 2001.
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[4] A. Ravi, et al., "An Optimally Transformer Coupled, 5 GHz Quadrature VCO in a 0.18μm Digital CMOS Process," *Dig. Symp. VLSI Circuits*, 2003, pp. 141-4.
[5] E. Hegazi, H. Sjöland, and A. A. Abidi, "A Filtering Technique to Lower LC Oscillation Phase Noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921–1930, Dec., 2001.

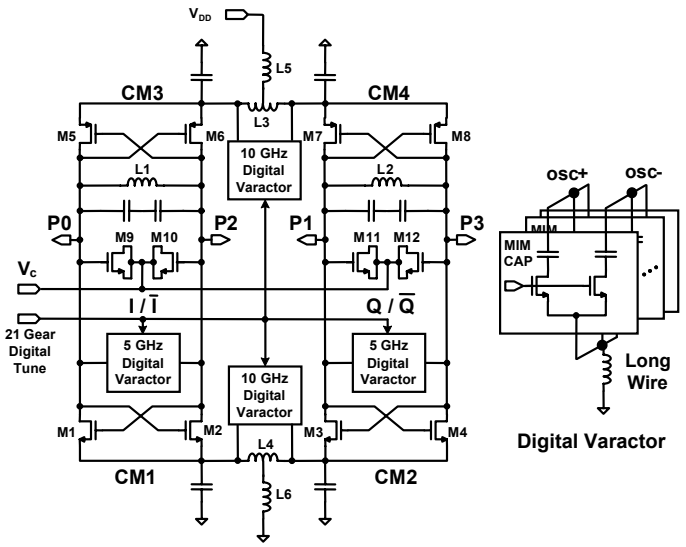

Figure 11.3.1: Energy-circulating QVCO.

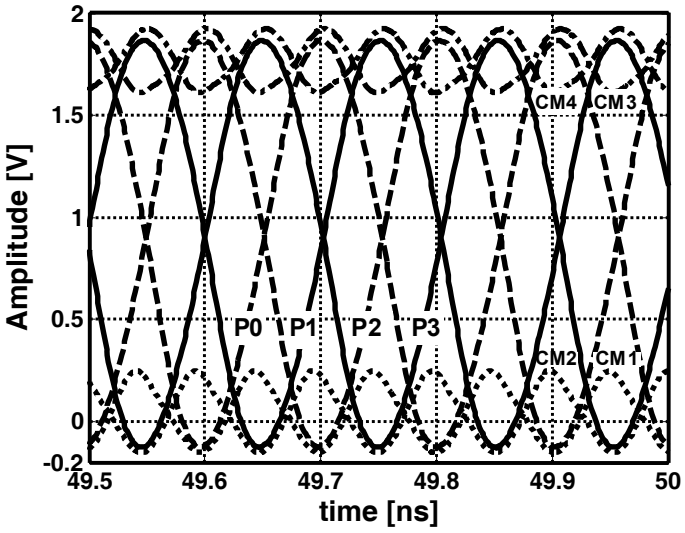

Figure 11.3.2: Oscillation waveform.

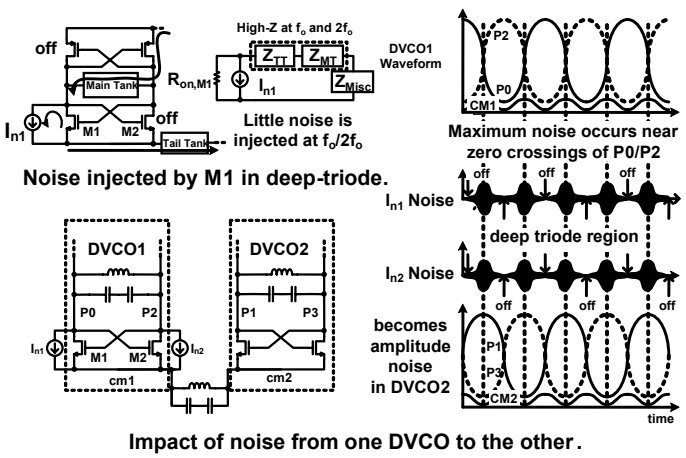

Figure 11.3.3: Noise injection and desensitization.

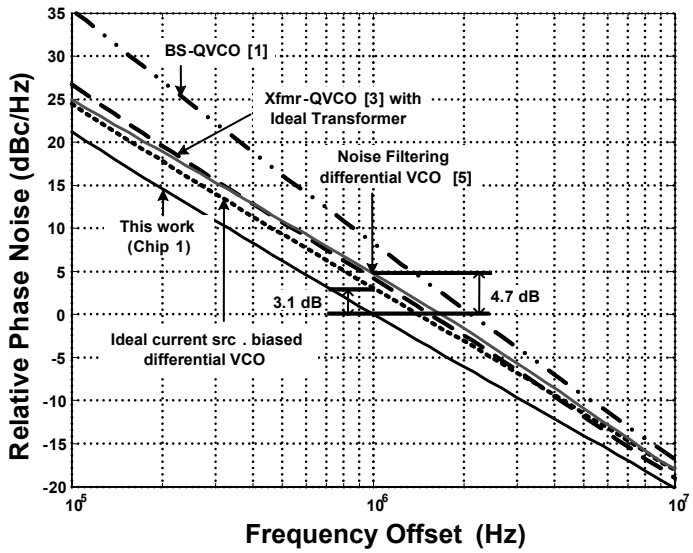

Figure 11.3.4: Simulated phase noise.

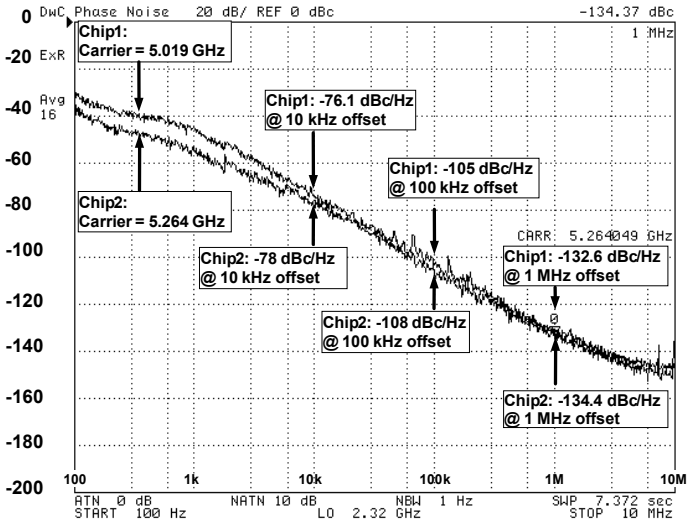

Figure 11.3.5: Measured phase noise.

	Chip 1	Chip 2
Technology	TSMC 0.18-µm CMOS	
Center Frequency	5.1 GHz	5.3 GHz
Tuning Range	17%	1%
VDD	1.8V	
Power Consumption	27.7 mW	20.7 mW
Phase Noise @ 1 MHz	-132.6 dBc/Hz	-134.4 dBc/Hz
FOM (2 MHz offset)	192 dB	196 dB
Chip Dimension	1.9 mm× 1.8 mm	1.9 mm× 1.6 mm

	Technology	Frequency	Tuning	FOM
[1]	0.35 µm	2.27 GHz	17 %	184
[2]	0.25 µm	1.88 GHz	12 %	185.5
[3]	0.25 µm	5 GHz	12 %	185
[4]	0.18 µm	5 GHz	20 %	186.2
This work	0.18 µm	5.1 GHz	17 %	192
This work	0.18 µm	5.3 GHz	1 %	196

Figure 11.3.6: Performance summary and comparison.

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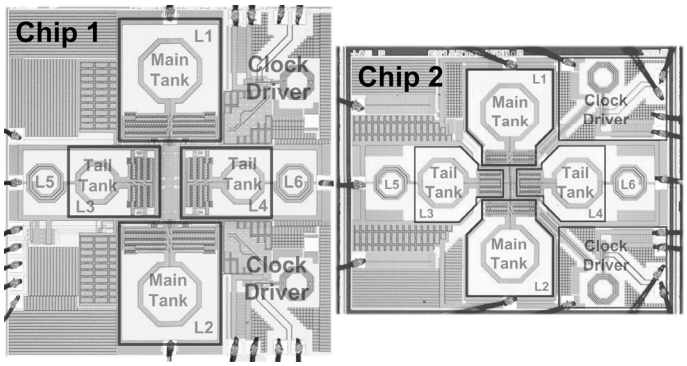

Figure 11.3.7: Chip micrographs.

